and first and second doped regions 304 and 306 are heavily doped (indicated by n+). In addition, first doped region 304 can be connected to a ground at node [312] 320. Those of ordinary skill in the art can readily recognize that first doped region 304 can also be connected to a voltage source or a power source. Second doped region 306 can be connected to an external bonding pad 312. Furthermore, since device 300 of Figure 3 includes no gate structure above the first and second doped regions 304 and 306, it is a gateless ESD protection device.

## IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 6, 7, 13, 17, 23, 27-29, and 33-35. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Amended) An electrostatic discharge (ESD) protection device comprising:

a substrate;

a first doped region formed in the substrate for connecting to a bonding pad; and

a second doped region formed in the substrate [and] for connecting to a power node, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the bonding pad and the power node through the substrate.

6. (Amended) An electrostatic discharge (ESD) protection device comprising:

a substrate;

a first doped region formed in the substrate for connecting to a bonding pad; and

a second doped region formed in the substrate [and] for connecting to a power node, wherein the second doped region is separated from the first doped region by only the substrate region, wherein an amount current flowing between the first and second doped regions is not

controlled by a voltage potential of a gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the bonding pad and the power node through the substrate.

7. (Amended) A gateless electrostatic discharge (ESD) protection device comprising:

a substrate;

a first doped region formed in the substrate for connecting to a bonding pad; and

a second doped region formed in the substrate [and] for connecting to a power node for receiving a power source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the bonding pad and the power node through the substrate.

13. (Amended) An electrostatic discharge (ESD) protection device comprising:

a substrate; and

an implant within the substrate, the implant including two implant regions spaced apart by only the substrate region, one of the two implant regions being connected to a bonding pad, another one of the two implant regions being connected to a power node, wherein the substrate comprises a first conductivity type and the two implant regions comprise a second conductivity type, wherein conductivity between the two implant regions is not controlled by voltage potential of a gate above the two implant regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the bonding pad and the power node through the substrate.

17. (Amended) An integrated circuit comprising:

a voltage source;

an external bonding pad; and

an electrostatic discharge (ESD) protection device connected between the external

bonding pad and the voltage source, the ESD protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the external bonding pad; and

a second doped region formed in the substrate and connected to the voltage source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the external bonding pad and the voltage source through the substrate.

23. (Amended) An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

a first electrostatic discharge (ESD) protection device connected between the first voltage source and the external bonding pad; and

a second ESD protection device connected between the second voltage source and the external bonding pad, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the second external bonding pad; and

a second doped region formed in the substrate and connected to the second voltage source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the external bonding pad and the second voltage source through the substrate.

27. (Amended) An integrated circuit comprising:

a voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node; and

an electrostatic discharge (ESD) protection device connected between the node and the voltage source, the ESD protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the external bonding pad; and

a second doped region formed in the substrate and connected to the voltage source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the external bonding pad and the voltage source through the substrate.

28. (Amended) An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node;

a first electrostatic discharge (ESD) protection device connected between the first voltage source and the node;

and

a second ESD protection device connected between the second voltage source and the node, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the second external bonding pad; and

a second doped region formed in the substrate and connected to the second voltage source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the external bonding pad and the second voltage source through the substrate.

29. (Amended) A semiconductor chip comprising:

a package having a plurality of pins; and

an electrostatic discharge (ESD) protection device connected to at least one of the pins,

the protection device comprising:

a substrate;

a first doped region formed in the substrate for connecting to the at least one of the pins; and

a second doped region formed in the substrate [and] for connecting to a power node, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the at least one of the pins and the power node through the substrate.

33. (Amended) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the at least one of the pins; and

a second doped region formed in the substrate [and] for connecting to a power node,

wherein the second doped region is separated from the first doped region by only the substrate region, wherein the protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the at least one of the pins and the power node through the substrate.

34. (Amended) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate; and

an implant within the substrate, the implant including two implant regions spaced apart by only the substrate region, one of the two implant regions being connected to the at least one of the pins, another one of the two implant regions being connected to a power node, wherein the substrate comprises a first conductivity type and the two implant regions comprise a second conductivity type, wherein conductivity between the two implant regions is not controlled by voltage potential of a gate above the two implant regions, wherein the protection device comprises no isolation structure between the first and second dope regions, and wherein only one path exists between the at least one of the pins and the power node through the substrate.

35. (Amended) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the at least one of the pins; and

a second doped region formed in the substrate [and] for connecting to a power node, wherein the second doped region is separated from the first doped region by only the substrate region such that an amount current flowing between the first and second doped regions is not